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Editor

A Combined Data and Power Management Infrastructure

For Small Satellites



Springer

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Foreword

Innovation is the key for success in technical fields and thus cannot be underestimated in space engineering domains working at the cutting edge of feasibility. Therefore, agile industry is continuously supporting innovative developments extending technical limits or abandoning classical design paths. It is particularly difficult to implement such innovative approaches straightforward in commercial satellite projects, in agency funded productive systems like operational Earth observation missions, or in navigation constellation programs.

The ideal platforms for “innovation verification” missions are governmental or academic technology demonstrator programs. These demonstrator programs allow for rapid prototyping of new capabilities and satellite architectures while keeping capital expenditures as low as possible.

Technology development partnerships between industry and academic institutions are extensively stressed and often cited. But for partnering in leading edge areas like the Combined Data and Power Management Infrastructure (CDPI), described in this book, such academic/Industry partnerships are extremely rare to find since they require substantial know-how, both on the industry and the university side.

However, once established, such cooperations provide a competitive edge for both the university as well as the industry partners. For industry the advantage is twofold because it allows the qualification of new space technology and in parallel students and Ph.D. candidates are educated to a knowledge level which is far above the normal standard for graduates.

For Astrium the University of Stuttgart has become a strategic technology partner over the past decade due to the extensive small satellite programs that have been established at their premises. These programs together with the state-of-the-art facilities at the Institute of Space Systems, hosted at the “Raumfahrtzentrum Baden-Württemberg”, go far beyond typical university CubeSat programs. The FLP satellite, for example, will qualify industry relevant flight hardware on board a university satellite for the first time in the German context.

For this reason Astrium has invested significantly in the development of this SmallSat program and in particular in this CDPI, both through direct sponsoring as well as through provision of manpower. The other consortium partners, Aeroflex,

4Links, Aeroflex Gaisler, Vectronic Aerospace, and HEMA Kabeltechnik, which all are close partners of Astrium, have also invested significant effort for development of their subsystems and have provided their SW/HW contributions at a university compatible cost basis.

For the German Aerospace Center this development is a key example of a successful industry/academic cooperation—a transcontinental one moreover. The technical product was developed in a 3.5 years timeframe, which is comparable with industry. The overall project concept with an experienced industry expert as team leader, industry suppliers for subsystems, and Ph.D. students complementing the team from the research side, the CDPI product testing and the integration into the satellite, proved to be a successful strategy.

This book is unique in that it presents in great detail a successful model for industry-university collaboration in the development of small satellites that aspire to cutting edge operational performance. We envision the beginnings of a worldwide trend for collaborative small satellite development with centers of excellence in Europe, North America, and Asia, with other nations also joining in the not too distant future.

December 2012

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Preface

The Combined Data and Power Management Infrastructure (CDPI) described in this book is a functional merging of a satellite Onboard Computer and a Power Control Unit. It was developed in the frame of the Small Satellites Program at the University of Stuttgart, Germany.

In 2009, the need became evident for a suitable Onboard Computer design for the small satellite FLP (also known as “Flying Laptop”). It had to meet the stringent performance, mass, volume, and power consumption constraints imposed by the 130 kg FLP satellite, with its full-featured ACS, diverse payloads, and complete CCSDS telecommand and telemetry standard compliance.

Thus one of my first tasks as senior engineer was to identify a design for an onboard computer which was required to be

- space proof w.r.t. radiation hardness and electromagnetic space conditions,
- compact enough for the target satellite platform (a cube of 60 x 70 x 80 cm),
- powerful enough to run a realtime operating system,
- suitable to support professional CCSDS-based satellite operations,
- and limited in power consumption.

Consumer electronic components for the onboard computer were out of the scope of this project considering the need for robustness against the space environment. Classic space industry OBC devices were not appropriate with regard to geometry and mass, much less cost considerations. The only realistic option was to find consortium partners from the space industry with expert knowledge in diverse fields who could supply the institute with Onboard Computer components—altogether forming a complete, redundant OBC. Thus the task was to define a completely modular, “LEGO® like” design which allowed the subcontracting of entire functional OBC boards to consortium partners. The overview of the achieved design solution is described in [Chap. 1](#).

The requirements on the OBC system, especially with respect to potential hardware failure robustness and the handling of different types of external analog and digital interfaces, led to a functional merging between OBC and the satellite’s Power Control and Distribution Unit (PCDU), resulting in a very innovative design—the so-called CDPI.

At end of the flight unit's development the consortium decided to provide a single consistent documentation of the developed CDPI Infrastructure. The technical overview should be available for other university students in a sort of mix between technical brochure and user guide. This book also might be of interest for future university or industry partners who intend to order in Stuttgart rebuilds/adaptations of the CDPI infrastructure or even the entire satellite bus for their missions.

December 2012

Prof. Dr.-Ing. Jens Eickhoff

Acknowledgments

This system development of a completely new and ultracompact Onboard Computer plus the functional merging of data and power management FDIR functions of both Onboard Computer (OBC), and Power Control and Distribution Unit (PCDU), would not have been possible without support from many sides to which we are indebted.

First of all in the name of the entire institute I would like to thank Evert Dudok, Director Astrium GmbH, Germany, for taking over the funding of the FM Processor-Boards and for their donation to the institute as in-kind sponsoring at the inauguration of the “Raumfahrtzentrum Baden-Württemberg” in 2011. Within Astrium I am also very much obliged to my site director in Friedrichshafen, Eckard Settelmeyer, and to my Section and Department Heads, Jörg Flemmig, and Volker Debus, for supporting this coaching activity in addition to my tasks at Astrium.

Secondly as overall system designer I am very much indebted to Hans-Peter Röser, the IRS institute director, who gave me plenty of range to conceptualize the overall system architecture, to find the consortium partners and negotiate with them, and to elaborate and finally verify the design at unit and system level. Last but not least it was him organizing the funding of all institute procured components.

Special thanks goes to the industry partners who joined this project, Aeroflex Colorado Springs, Inc. CO USA, Aeroflex Gaisler AB Sweden, 4Links Ltd. UK, Vectronic Aerospace GmbH and HEMA Kabeltechnik GmbH & Co. KG, Germany. It is absolutely non-standard that a university project is supported so intensively by industrial global players.

In 2009, I had just taken over the role of the engineering coach of the FLP satellite and was standing empty-handed, lacking a convincing OBC solution for the satellite. My first idea was to upgrade one of the Aeroflex Gaisler development boards. I contacted Jiri Gaisler at the DASIA conference in 2009 and herewith I express my gratitude to him for handing over my problem to Aeroflex Inc. USA. They were just developing a Single Board Computer based on the LEON3FT chip UT699. From this initial contact, the fruitful cooperation between the university and Aeroflex evolved.

Concerning the OBC development the university team is indebted to Aeroflex and their German distributor Protec GmbH, Munich, for guiding us through the formalisms of the procurement of the CPU boards as being ITAR products. Aeroflex helped us to fill out all relevant forms and explained the “dos and don’ts” concerning, shipment, and publishing rules under ITAR. The Processor-Boards were provided under Technical Assistance Agreement TA-6151-10. The author’s team is also indebted to the Aeroflex management and particularly to Tony Jordan for granting their chief developer Sam Stratton the permission to participate in this book and for reviewing the Aeroflex chapter concerning ITAR compliance.

For the publishing of this book the author’s team thanks Mrs. Sterritt-Brunner and Dr. Christoph Baumann and the Springer publishing team for their assistance.

Last but not least as project manager of the CDPI, I do not want to forget to express my gratitude and respect to the highly motivated FLP team of Ph.D.s and students and in particular to those Ph.D.s which became co-authors in this book.

December 2012

Prof. Dr.-Ing. Jens Eickhoff

Donation for Life

In 2011, during the CDPI development, the 10-year-old daughter of one of the authors was diagnosed to be suffering from a breakdown of blood cell production in the bone marrow—a variant of blood cancer. She luckily could be saved and recovered by means of a bone marrow transplant. Due to this experience the authors decided to sponsor with the royalties of this book the German and international bone marrow donor's database:

DKMS Deutsche Knochenmarkspenderdatei gemeinnützige Gesellschaft mbH
Phone: +49-(0)7071-9430

German Website: <https://www.dkms.de/>

US Website: <http://www.dkms-americas.org/>



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Abbreviations

General Abbreviations

a.m.	Above mentioned
cf.	Confer
i.e.	Id est (that is)
w.r.t.	With respect to

Technical Abbreviations

ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AIT	Assembly, Integration, and Test
ASIC	Application-Specific Integrated Circuit
ASM	Attached Synchronization Marker
AWG	American Wire Gauge
BBM	Breadboard Model
BCH	Bose–Chaudhuri–Hocquenghem
BCR	Battery Charge Regulator
BoL	Begin of Life
CAD	Computer-Aided Design
CADU	Channel Access Data Unit
CC	Combined-Controller
CCSDS	Consultative Committee for Space Data Systems
CD	Clock Divider
CDPI	Combined Data and Power Management Infrastructure
CE	Convolutional Encoder
CE	Circuit Enable/Chip Enable
CL	Coding Layer
CLCW	Command Link Control Word
CLTU	Command Link Transfer Unit
CMOS	Complementary Metal Oxide Semiconductor
CPDU	Command Pulse Decoding Unit

CPU	Central Processing Unit
DEI	DSU/Ethernet Interface
DMA	Direct Memory Access
DoD	Depth of Discharge
DOM	De-Orbiting Mechanism
DRAM	Dynamic Random Access Memory
DSU	Debug Support Unit
ECSS	European Cooperation on Space Standardization
EDAC	Error Detection and Correction
EEPROM	Electrically Erasable PROM
EM	Engineering Model
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EPPL	European Preferred Parts List
ESA	European Space Agency
ESD	Electrostatic Discharge
FDIR	Failure Detection, Isolation, and Recovery
FIFO	First-In-First-Out
FM	Flight Model
FOG	Fiberoptic Gyro
FPGA	Field Programmable Gate Array
FRAM	Ferroelectric Random Access Memory
GPIO	General Purpose Input/Output
GPS	Global Positioning System
GSE	Ground Support Equipment
HF	High Frequency
HK	Housekeeping
HPC	High Priority Command
HW	Hardware
I/O	Input/Output
IADC	United Nations Inter-Agency Space Debris Coordination Committee
IC	Integrated Circuit
IF	Interface
IIC	Inter-Integrated Circuit Bus
IRS	Institut für Raumfahrtssysteme, Institute of Space Systems, University of Stuttgart, Germany
ITAR	International Traffic in Arms Regulations
ITU	International Telecommunication Union
JTAG	Joint Test Actions Group
LCL	Latching Current Limiter
LEOP	Launch and Early Orbit Phase
LISN	Line Impedance Stabilization Network
LTDN	Local Time of Descending Node
LVDS	Low Voltage Differential Signaling
MAP-ID	Multiplexer Access Point Identifier

MCM	Multi-Chip Module
MCS	Mission Control System
MGM	Magnetometer
MGT	Magnetotorquer
MRAM	Magnetoresistive Random Access Memory
MSI	Medium-Scale Integration
MTQ	Magnetotorquer
NASA	National Aeronautics and Space Administration
NRZ-L	Non-Return-to-Zero Level
NRZ-M	Non-Return-to-Zero Mode
NVRAM	Non-Volatile RAM
OBC	Onboard Computer
OBSW	Onboard Software
OS	Operating System
PCB	Printed Circuit Board
PCDU	Power Control and Distribution Unit
PFM	Protoflight Model
PLOC	Payload Controller—“Payload Onboard Computer”
POR	Power On Reset
PPS	Pulse Per Second
PROM	Programmable Read-Only Memory
PSR	Pseudo Randomizer
PSU	Power Supply Unit
PUS	ESA Packet Utilization Standard
QA	Quality Assurance
RAM	Random Access Memory
RF	Radio Frequency
RF-SCOE	Radio Frequency Special Check-Out Equipment
RISC	Reduced Instruction Set Computer
RIU	Remote I/O Unit (of an OBC)
ROM	Read Only Memory
RTOS	Realtime Operating System
RTS	Realtime Simulator
RWL	Reaction Wheel
S/C	Spacecraft
SA	Solar Array
SBC	Single Board Computer
SCID	Spacecraft Identifier
SCOE	Special Checkout Equipment
SDRAM	Synchronous Dynamic Random Access Memory
SEL	Single Event Latch-up
SEU	Single-Event Upset
SIF	Service Interface
SMD	Surface Mounted Device
SoC	System on Chip

SoC	Battery State of Charge
SPARC	Scalable Processor Architecture
SpW	SpaceWire
SRAM	Static Random Access Memory
SSO	Sun-Synchronous Orbit
SSRAM	Synchronous Static Random Access Memory
STR	Star Tracker
SW	Software
TAA	Technical Assistance Agreement
TC	Telecommand
TCC	Telecommand Channel Layer
TF	Transfer Frame
TID	Total Ionizing Dose
TM	Telemetry
TMR	Triple Module Redundancy
TTL	Transistor–Transistor Logic
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
VC	Virtual Channel
VCID	Virtual Channel Identifier
WS	Workstation